

What Is Claimed Is:

1 1. A method for verifying optimization of processor link
2 for a system comprising a Northbridge, a bus coupled between a
3 CPU and the Northbridge, and a Southbridge, the method
4 comprising the following steps:

5 setting an initial bus width and an initial bus frequency
6 of the bus coupled between the CPU and the
7 Northbridge, wherein the bus operates at the initial
8 bus width and the initial bus frequency;

9 generating a read request to read the Southbridge;

10 output of a bus disconnection signal by the Southbridge to
11 disconnect the CPU and the Northbridge when the
12 Southbridge receives the read request, initializing
13 a timer for calculating an elapsed time value and
14 outputting an optimization verification signal with
15 a first voltage level;

16 output of a bus connection signal by the Southbridge when
17 the elapsed time value reaches a predetermined value
18 and transforming the voltage level of the
19 optimization verification signal to a second voltage
20 level; and

21 reconnection of the CPU and the Northbridge by the bus
22 according to the bus connection signal, wherein the
23 bus operates at another bus operating bus width and
24 another bus operating frequency.

1 2. The method for verifying optimization of processor
2 link as claimed in claim 1, wherein the bus is a lightning data
3 transport bus.

1 3. The method for verifying optimization of processor
2 link as claimed in claim 1, wherein the bus is a hyper-transport
3 bus.

1 4. The method for verifying optimization of processor
2 link as claimed in claim 1, further comprising the step of
3 setting an optimized bus operating bus width and an optimized
4 bus operating frequency of the bus.

1 5. The method for verifying optimization of processor
2 link as claimed in claim 4, wherein the bus operates at the
3 optimized bus operating bus width and the optimized bus
4 operating frequency when the CPU and the Northbridge are
5 reconnected.

1 6. The method for verifying optimization of processor
2 link as claimed in claim 1, wherein the bus disconnection signal
3 and the bus connection signal are output by a single output
4 terminal.

1 7. The method for verifying optimization of processor
2 link as claimed in claim 1, wherein the bus disconnection signal
3 and the bus connection signal are generated by asserting and
4 de-asserting a signal output by the Southbridge.

1 8. The method for verifying optimization of processor
2 link as claimed in claim 1, wherein the optimization
3 verification signal is output by a signal level detection
4 circuit.

1 9. The method for verifying optimization of processor
2 link as claimed in claim 1, wherein the signal level detection

3 circuit comprises a flip-flop and an OR logic gate coupled to
4 the flip-flop, the flip-flop outputs the optimization
5 verification signal with the first voltage level when the
6 Southbridge outputs the bus disconnection signal, and outputs
7 the optimization verification signal with the second voltage
8 level when the Southbridge outputs the bus connection signal

1 10. The method for verifying optimization of processor
2 link as claimed in claim 8, wherein the signal level detection
3 circuit is coupled to the output terminal of the Southbridge.

1 11. The method for verifying optimization of processor
2 link as claimed in claim 8, wherein the signal level detection
3 circuit is coupled to the input terminals of the CPU or the
4 Northbridge.

1 12. A method for verifying optimization of processor link
2 for a system comprising a Northbridge, a bus coupled between the
3 CPU and the Northbridge, and a Southbridge, the method
4 comprising the following steps:

5 setting an initial bus width, an initial bus frequency, a
6 bus operating bus width and a bus operating frequency
7 of the bus coupled between the CPU and the
8 Northbridge, wherein the bus operates at the initial
9 bus width and the initial bus frequency;

10 setting an optimized bus operating bus width and an
11 optimized bus operating frequency of the bus;

12 generating a read request to read the Southbridge;

13 output of a bus disconnection signal by the Southbridge to
14 disconnect the CPU and the Northbridge when the
15 Southbridge receiving the read request,

16 initializing a timer for calculating an elapsed time
17 value and outputting an optimization verification
18 signal with a first voltage level;
19 output of a bus connection signal by the Southbridge when
20 the elapsed time value reaches a predetermined value
21 and transforming the voltage level of the
22 optimization verification signal to a second voltage
23 level; and
24 reconnection of the CPU and the Northbridge by the bus
25 according to the bus connection signal, wherein the
26 bus operates at the optimized bus operating bus width
27 and the optimized bus operating frequency.

1 13. The method for verifying optimization of processor
2 link as claimed in claim 12, wherein the bus is a lightning data
3 transport bus.

1 14. The method for verifying optimization of processor
2 link as claimed in claim 12, wherein the bus is a hyper-transport
3 bus.

1 15. The method for verifying optimization of processor
2 link as claimed in claim 12, wherein the bus disconnection signal
3 and the bus connection signal are output by a single output
4 terminal.

1 16. The method for verifying optimization of processor
2 link as claimed in claim 12, wherein the bus disconnection signal
3 and the bus connection signal are generated by asserting and
4 de-asserting a signal output by the Southbridge.

1 17. The method for verifying optimization of processor
2 link as claimed in claim 12, wherein the optimization
3 verification signal is output by a signal level detection
4 circuit.

1 18. The method for verifying optimization of processor
2 link as claimed in claim 17, wherein the signal level detection
3 circuit comprises a flip-flop and an OR logic gate coupled to
4 the flip-flop, the flip-flop outputs the optimization
5 verification signal with the first voltage level when the
6 Southbridge outputs the bus disconnection signal, and outputs
7 the optimization verification signal with the second voltage
8 level when the Southbridge outputs the bus connection signal

1 19. The method for verifying optimization of processor
2 link as claimed in claim 12, wherein the signal level detection
3 circuit is coupled to the output terminal of the Southbridge.

1 20. The method for verifying optimization of processor
2 link as claimed in claim 12, wherein the signal level detection
3 circuit is coupled to the input terminals of the CPU or the
4 Northbridge.